Chapter 8

The UNIVAC system[1]

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Organization of the UNIVAC system

In March 1951, the first UNIVAC[2] system formally passed its acceptance tests and was put promptly into operation by the Bureau of the Census. Since the UNIVAC is the first computer which can handle both alphabetic and numerical data to reach full-scale operation so far, its operating record and a review of the types of problems to which it has been applied provide an interesting milestone in the ever-widening field of electronic digital computers.

The organization of the UNIVAC is such that those functions which do not directly require the main computer are performed by separate auxiliary units each having its own power supply. Thus the keyboard to magnetic tape, punched card to magnetic tape and tape to typewritten copy operations are delegated to auxiliary components.

The main computer assembly includes all of those units which are directly concerned with the main or central computer operations. A block diagram of this arrangement is shown in Fig. 1. All of the elements shown are contained within the central computer casework except the supervisory control desk (*SC*) and the Uniservos,[2] to which the lines in the upper right section of the diagram connect.

The supervisory control, in addition to all the necessary control switches and indicator lights, contains an input keyboard. Also cabled to the supervisory control is a typewriter which is operable by the main computer. By means of these two units, limited amounts of information can be inserted or removed either at the will of the operator or by the programmed instructions.

The input-output circuits operate on all data entering or leaving the computer. The input and output synchronizers properly time the incoming or outgoing data for either the Uniservos (tape devices) or the supervisory control devices. The input and output registers (*I* and *O*) are each 60 word (720 characters) temporary storage registers which are intermediate between the main computer and the input-output devices.

The high-speed bus amplifier is a switching central through which all data must pass during transfer between any arithmetic register and the main memory or between the memory and the input-output registers. The arithmetic registers are shown along the bottom of diagram each connected to the high speed bus system.

The *L*-, *F*-, *X*-, and *A*-registers are each of one word or 12-character capacity and are directly concerned with the arithmetic operations. The *V*- and *Y*-registers are of 2- and 10-word capacity, respectively. They are used solely for multiple word transfers within the main memory. Associated with the arithmetic registers are the algebraic adder (*AA*), the comparator (*CP*), and the multiplier-quotient counter (*MQC*).

Addition-subtraction instructions

The addition-subtraction operations are performed in conjunction with the comparator since all numerical quantities are absolute magnitudes with an algebraic sign attached. Before either an addition or subtraction is performed, the two quantities, one already in the *A*-register and the other either from the memory or from the *X*-register, depending upon the particular instruction, are compared for magnitude and sign. The adder inputs can then be switched so as always to produce a noncomplemented result for any operation. The choice of adder input arrangement is therefore under the control of the comparator. The comparator also determines the proper sign for the result according to the usual algebraic rules.

One additional function performed by the comparator for addition and subtraction is to control the complementer. This determination is based upon which operation (+, or −) is indicated, and, whether the signs are like or unlike. For a subtract instruction, the sign of the subtrahend is reversed before entering the comparator. The comparator then compares the signs of the quantities in order to determine whether the two quantities are subtracted or added.

Multiplication instruction

The multiplication process requires the services of the adder, the comparator, the multiplier-quotient counter and the four arithmetic registers. During the first step of multiplication the *X*-reg-

[1] *AIEE-IRE Conf.*, 6–16, December, 1951.
[2] Registered trade mark.

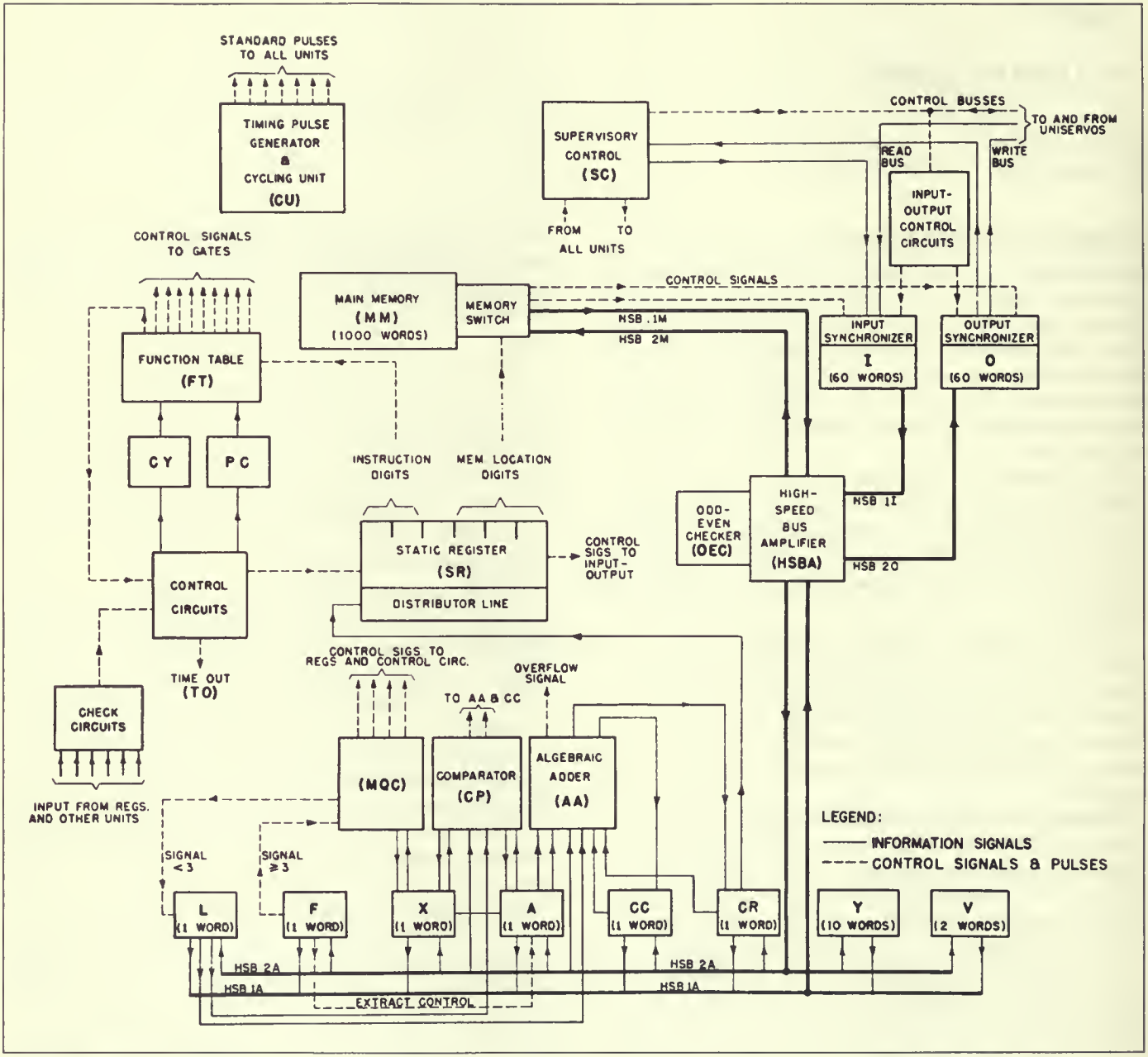

Fig. 1. Block diagram of UNIVAC.

ister receives the multiplier from the memory and the comparator determines the sign of the final product by comparing the signs of the multiplier and multiplicand. During the next three steps the multiplicand, which has been stored in the *L*-register by some previous instruction, is transferred three times to the *A*-register through the algebraic adder. The result, three times the multiplicand, is then stored in the F-register. During the next 11 steps of multiplication, the successive multiplier digits, beginning with the least significant, are transferred from the *X*-register to the multiplier-quotient counter. The multiplier-quotient counter then determines whether each particular multiplier digit is less than three, or greater than or equal to three.

If the former, the *L*-register releases the multiplicand to the *A*-register via the adder, and the multiplier-quotient counter is stepped downward one unit. If the multiplier digit is equal to or greater than three, the multiplier-quotient counter sends a signal to the *F*-register which releases three times the multiplicand to the *A*-register and the multiplier-quotient counter is stepped three times. Thus a multiplier digit of seven would be processed as two transfers from the *F*-register to the *A*-register and one transfer from the *L*-register to the *A*-register, or a total of three transfers.

When the multiplier-quotient counter reaches zero, the next multiplier digit is brought in from the *X*-register, while the *A*-register, containing the first partial product, is shifted one position to the right.

During the final step of multiplication, the sign is attached to the product which has been built up in the *A*-register. One of the several available multiplication instructions causes the least significant digits, as they are shifted beyond the limits of the *A*-register, to be transferred to the *X*-register where they replace the multiplier digits as they are moved to the multiplier-quotient counter. Thus 22 place products can be obtained as well as 11 place.

Division instruction

The division operation is performed by a nonrestoring method. The divisor is stored in the *L*-register by some previous instruction and the dividend is brought from the memory and put in the *A*-register during the first step of the division instruction. As in multiplication, the signs of the two operands are compared in the comparator at this time and the sign of the quotient is then stored in the comparator pending completion of the division operation. The principal stages of division consist of transferring the divisor from the *L*-register to the *A*-register through the complementer and adder as many times as required to produce a quantity less than zero in the *A*-register, the dividend having been first shifted one position to the left. The multiplier-quotient counter counts each transfer, thereby building up the first quotient digit. As soon as the quantity in the *A*-register, (neglecting its original sign) goes negative, the digit in the multiplier-quotient counter, not counting the transfer which causes the remainder to go negative, is transferred to the *X*-register and the remainder in the *A*-register is shifted one place to the left. The divisor is then added to the *A*-register until the quantity becomes positive. This time the multiplier-quotient counter must give the complement of the number of transfers for the real quotient digit. Special complementing read-out gates provide this method of interpreting the multiplier-quotient counter.

The *X*-register therefore collects the quotient, digit by digit, from the multiplier-quotient counter until the full 11 digits have been obtained. The quotient is then transferred to the *A*-register and the sign from the comparator (*CP*) is affixed during the final stage of the divide instruction.

The other internal operations of the UNIVAC include many transfer instructions by which words may be moved among the registers and memory with and without clearing, the extraction instruction by which certain digits of a word may be extracted into another word according to the parity of the corresponding digits of an extractor word; shift instructions; and special control instructions such as breakpoint, transfer of control, (explained in subsequent paragraphs) and stop.

Basic operating cycle

The basic operating cycle of the UNIVAC is founded upon single address instructions which specify the memory location of one word. In the case of the arithmetic instructions which require two operands, one of the operands must be moved into the proper register by some previous instruction. In order to control the sequence of instructions, a special counter, called the control counter (*CC*), retains the memory location from which the succeeding instruction word is to be obtained. Each time a new instruction word is received from the memory, the quantity in the control counter is passed through the adder where a unit is added to it. Therefore the normal sequence is to refer to successive memory locations for successive instruction words. Initially the control counter is cleared to zero and the first group of instructions must, therefore, be placed in memory locations from zero upward. A transfer of control instruction enables the programmer to change the control counter reading whenever desired and thus shift from one sequence to another. After a transfer of control takes place, the new number in the control counter is increased by unity each time a new instruction word is obtained from the memory.

Transfer of control instructions

The transfer of control instructions are of three types, the unconditional transfer which changes the control counter reading without question, and two conditional instructions which require that either equality or a specific inequality exists between the words in the *A*-register and the *L*-register. In the former case the quantities must be identical for transfer of control to occur and in the latter the quantity in the *A*-register must be greater than the quantity in the *L*-register for the control counter reading to be changed.

Since the UNIVAC can handle alphabetic as well as numerical data, these conditional transfer instructions are as useful for alphabetizing as they are to determine if a certain iterative arithmetic process has been performed often enough to come within specified numerical tolerances.

Control register

Since six characters (intermixed alphabetic and numerical) are sufficient to specify an instruction and there are 12 characters per word, each instruction word can represent two independent instructions. A 1-word register, called the control register (*CR*), has been provided which stores each instruction word as it comes from the memory. Thus one memory referral is sufficient for a pair of instructions and the control register stores both halves so that the second instruction is available as soon as the first has been completed.

The general term control circuits includes all those elements which work together to process the instruction routine. As each instruction word reaches the control register, the first half of it is passed immediately into the static register (*SR*). The static register drives the main function table and memory switch. The instruction digits are translated by the function table into the appropriate control signals for the instruction called for. The memory switch selects the location called for by the memory location digits and opens the proper memory channel to the high-speed bus system at the proper time. Since the memory is constructed of 100 channels, each holding ten words, the memory switch is a combination of spatial and temporal selection.

Cycle counter

Implicit within each instruction, as translated by the function table, is an ending signal which causes the computer to move on to the next instruction. The key to this sequence is the cycle counter (*CY*), which is advanced by the ending pulse. The cycle counter is a 2-stage 4-position counter, which is connected into the function table. By virtue of this relation, *CY* develops signals in addition to those developed by the instruction, which, for example, can cause the control register to transfer the second half of the instruction word into the static register when the first half has been completed. Similarly, after the second half instruction is finished the cycle counter causes the reading of the control counter to pass into the memory location section of the static register and thus cause the next instruction word to be transferred from the memory to the control register. When the word reaches the control register, the cycle counter also causes the control counter reading to be increased by unity. The four cycles are designated by the first four Greek letters α (transfer *CC* to *SR*), β (transfer memory to *CR*), γ (perform first instruction), and δ (perform second instruction).

Program counter

The multistage instructions, such as multiplication, are guided through their various steps by the program counter (*PC*). The program counter has four stages or 16 positions. All multistage instructions can be performed within this number of steps.

Checking circuits

The checking circuits of the UNIVAC are of two main types, odd-even checkers and duplicated equipment with comparison circuits. The odd-even checker depends upon the design of the pulse code used within the computer. This code provides seven pulse positions for every character. Six of the seven positions are significant as the actual code while the seventh is the odd-even channel. If the number of pulses or ones within the first six channels of any character is even, a one is placed in the seventh channel to make the total odd. Thus, the total number of ones across the seven channels is always odd. By means of a binary counter and a few gates, an odd-even checker has been constructed which examines every seven pulse group which passes through the high speed bus amplifier. In this connection, mention must be made of the periodic memory check which interrupts operation every five seconds to pass the entire contents of the memory over the high speed bus system and, consequently, through the odd-even checker. Any discrepancy is immediately signalled to the supervisory control and further operation ceases.

The duplicated equipment type of checking consists of duplicating the most essential part of the arithmetic circuits and their controls and producing simultaneously independent results, which can then be compared for equality. For this type of checking, the *A*-, *F*-, *X*-, and *L*-registers, algebraic adder, comparator, multi-

plier-quotient counter, and the high speed bus amplifier are duplicated.

The memory is not duplicated, but is checked by the periodic memory check mentioned previously. Various sections of the control circuits are duplicated such as the program counter and cycle counter.

Timing pulse generator and cycling unit

The timing pulse generator and cycling unit (*CU*) are the source of the basic timing signals throughout the computer. The timing pulses occur at 2.25 megacycles per second. The cycling unit subdivides this rate into the character rate and word rate. The character rate is one seventh of the basic pulse rate since there are seven pulses for each character. There are 12 characters per word but space for a 13th character is included in a word time and is called the space between words. This time is used for switching purposes.

The cycling unit, therefore, develops the word signals at $\frac{1}{7} \times \frac{1}{13}$ or $\frac{1}{91}$ of the basic pulse rate. Within the cycling unit (*CU*) are numerous duplications and comparisons to ensure complete reliability.

Input-output circuits

The operation of the input-output system is dovetailed as efficiently as possible with the operation of the arithmetic circuits. Whenever possible, parallel operations are allowed to proceed so as to minimize the time lost on internal operation while the slower input-output operations are taking place.

The principal input-output instructions are handled in a manner identical to that for the internal operations, except that now the function table develops signals which bring the input-output control circuits into operation. The information supplied to the input-output control circuits by the function table includes the following:

1 Which of the ten possible Uniservos is being called on

2 Whether it is a read or write, that is, an input or output operation

3 If it is "read," the direction in which the tape is to move

The input-output control circuits, therefore, begin by testing whether or not the Uniservo indicated now is in use or not. If it is already in use, everything else waits until that Uniservo is free. Next, the input-output control circuits test to determine whether the Uniservo selected last moved backward or forward. If the previous direction does not agree with the new direction called for, the input-output control circuits generate the proper signals to prepare the Uniservo to move in the opposite direction. If the instruction is to rewind a Uniservo, the input-output control circuits then direct the center drive of the selected Uniservo to rewind the tape to the beginning and stop.

As soon as the instruction has proceeded to the point where the input-output control circuits need no further information from the function table, the instruction ending signal is generated and the internal circuits proceed to the next instruction, even while the reading, writing or rewinding continues. The UNIVAC can process an input, an output and several rewind operations while simultaneously carrying on internal computation.

So far the method by which the words are transferred from the *I*-register to the memory has not been mentioned. This operation is combined with certain read instructions in a manner not immediately obvious. There are two instructions which read from the tape to the *I*-register, one causing the tape to move forward, the other causing it to move backward. There are two other input instructions similar to those just mentioned, but they have the additional operation of first reading from the *I*-register to the memory and then reading a new group of 60 words from tape into the *I*-register. Thus the first type of input instruction reads from tape to the *I*-register only. It must be followed by the second type of instruction in order first to clear the *I*-register and then read in the second block of 60 words.

The output instructions do not operate in this way but instead read directly from memory to the *O*-register and then to the tape as one instruction.

A third type of checking circuit occurs in the input-output control circuits which counts the number of characters transferred from the tape in each block. Since there must always be 720 characters per block, the 720 checker signals any discrepancy to the supervisory control.

One other phase of the input-output operation concerns the two supervisory control input-output instructions. One of them permits a single word to be typed in from the input keyboard and the other causes a single word to be typed out automatically.

Auxiliary equipment

The two principal auxiliary devices mentioned earlier were the Unityper,[1] which converts keyboard operations to tape recording, and the Uniprinter,[1] which converts magnetic recording to typewritten copy.

[1]Registered trade mark.

Unityper. A simple block diagram of the Unityper is shown in Fig. 2. Each keyboard operation pulses the input to an encoding function table which, in turn, drives the appropriate heads for recording the particular combination on the tape. Simultaneously, the same pulse triggers a motor delay flop which operates the tape motor for an interval sufficient to move the tape across the head for the distance required to record one character. However, there is a punched paper loop system associated with the Unityper for the purpose of providing the typist with various guideposts individually set up for each problem. The loop control system serves three distinct control functions. First, it allows the programmer to set up various numbers of characters for the individual items being entered for a given problem. If the typist ever enters other than the specified number of characters, the loop control signals an error. Although the basic word length is 12 characters, the programmer may subdivide or group the words to suit any length of item. The loop can then be punched with what are called "force check" punches. Whenever the typist completes a correctly entered item, she must operate a release key before entering the next item. If the forced check is released too early an error is created, or if an additional character is typed after the forced check should have been released, an error is similarly indicated.

The second function of the loop is to control the erase operation. The erase operation is the only way in which an error can be recalled. When the erase key is operated, the loop and tape are both stepped backward until a stop punch (usually associated with each forced check) is encountered. Thus the entire erroneous item is erased, and at a much higher rate than that at which the backspace key can be operated. The backspace, incidentally, cannot cancel an error indication, but it can be used to correct a wrongly typed character if the typist recognizes it.

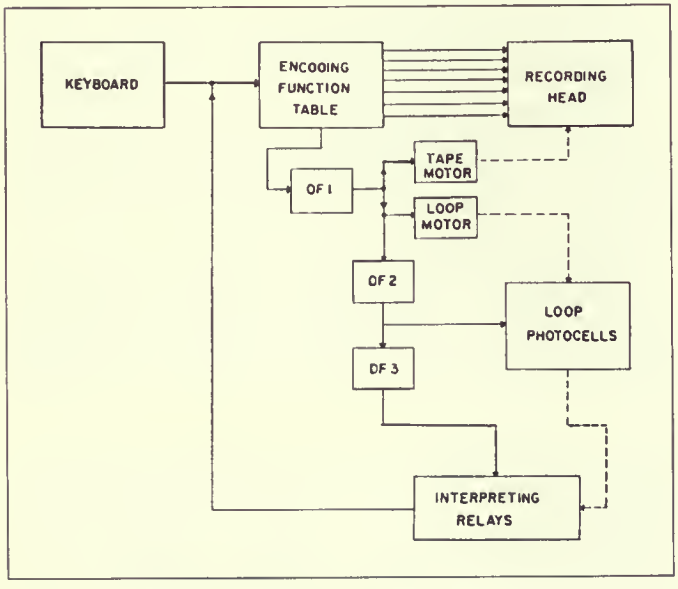

Fig. 2. Simplified block diagram of Unityper.

The third function of the loop system is to enter, automatically, various fill-in characters. Under one such system of operation, the loop control records the characters only at the behest of the operator. This function is useful where individual entries, such as personal names, do not fill out all of the space allotted. The other operation is fully automatic in which the loop assumes full control to record, for example, a group of fill-in characters later to be replaced by computed data within the central computer.

The block diagram therefore shows the loop motor connected to the same delay flop that steps the tape motor. The same signal which moves the two motors also sets a second delay flop (*DF2*) which produces a delayed probing pulse. The probing pulse examines the paper loop photoelectrically for the new combination. A third delay flop (*DF3*) produces another probing pulse after the relays associated with the loop photocells have had time to set up. If any automatic function is indicated by the photocells, the probing pulse passes through the interpreting relays, enters the encoding function table to generate the fill-in characters, and thus starts the cycle over again. All automatic functions take place at about 22 characters per second.

Numerous odd-even checks are introduced in the Unityper to provide checks on tape and loop motion and on the recorded code combination.

Uniprinter. The Uniprinter is shown in simplified block diagram in Fig. 3. Its operation is a simple cycle which is initiated by a start button. The start button triggers the motor flip-flop (*MFF*). The motor pulls the tape across the reading head until a combination is detected. The presence of pulses on any of the seven lines between the reading head and the relay decoding function table is sufficient to restore the motor flip-flop (*MFF*) and stop the tape motion. Simultaneously a print delay flop (*DF1*) is triggered. During the delay flop interval, the decoding relays are given time to set up. When the delay flop recovers, a pulse is sent through the relay table which reappears at one of the typewriter magnetic actuators. As the typebar reaches the platen, a printer action switch (*PAS*) is operated which pulses the motor flip-flop and starts a new search for the next character on the tape. The odd-even properties of the UNIVAC pulse code are utilized for checking purposes.

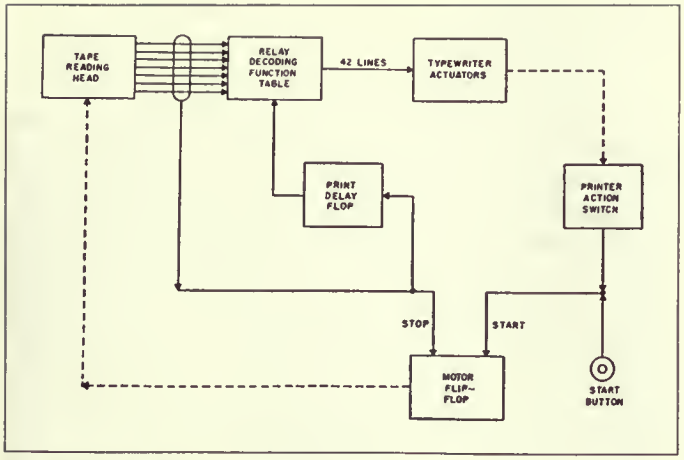

Fig. 3. Simplified block diagram of Uniprinter.

Engineering aspects

The entire UNIVAC system is constructed of circuits which are as conservative as is consistent with the desired reliability and speeds of operation. The circuits have been designed as building blocks and the entire computer is constructed around these blocks.

One of the most important of these blocks is the pulse reshaping circuit which consists of a timing pulse gate and a fast acting flip-flop which generates the pulse envelope equivalent of the gated timing pulses. Two polarities of timing pulse are used, the one being capable of tripping the flip-flop into one state, the other polarity of tripping it to the other state. As a deteriorated pulse envelope is applied to the timing pulse gate input, either one or the other polarity of pulse is always gated. The flip-flop therefore produces a sharpened and correctly timed output waveform.

The gating and switching circuits in the central computer are constructed of germanium crystal diodes, which include the main and subordinate function tables.

The registers are all circulating delay type using a mercury tank of one, two, or ten word-times of delay, except the static register. The latter is composed of 27 flip-flops which are required to maintain the static signals applied to the function tables, for at least an entire word-time.

The switching time allowed by the seven pulse-times of the space between words is, in general, not sufficient for a new function table excitation to stabilize. Therefore the time-out system used successfully in the BINAC, also is employed in the UNIVAC. Whenever an ending pulse is generated, or any other pulse which indicates that a new set of control signals are required from the function table, an interval of one word-time is introduced to allow the function table signals to reach equilibrium. The time-out interval is controlled by a single fast-acting flip-flop. All gates attached to the function table signals which are critical as to opening and closing can be inhibited by the time-out flip-flop during time out. Regardless of the presence of the function table signals, the gate does not operate until the time-out flip-flop releases it. Thus, the burden of speed imposed by the short space between words has been shifted to a single flip-flop which can accommodate the needs of the entire computer.

The UNIVAC uses the excess-three pulse code system which requires a second binary adder after the main binary adder in order to provide the excess-three correction after each addition. On the other side of the ledger, the complementing operation for subtraction and division is very much simplified, since the substitution of ones for zeros and vice versa is sufficient to form a complement. The excess-three part of the pulse code occupies the four least significant digit positions. The next two positions beyond the excess-three digits are used as zone indicators. When these digits are both zero, the last four positions are interpreted as a numerical quantity; when nonzero, an alphabetic or punctuation symbol is indicated. The seventh channel is the check pulse channel.

The adder is provided with an alphabetic bypass circuit which allows an alphabetic letter to enter one input and emerge unscathed provided a numeral enters the other input. Thus additive numerical constants can be combined with instruction words to adjust the memory location part of an instruction without affecting the alphabetic instruction symbols.

The power supply for the computer is separately housed. It can be placed any reasonable distance from the central computer. Almost all rectification is done by dry disc rectifiers. The power supply provides all a-c and d-c potentials to the central computer, supervisory control, directly-connected printer, and the Uniservos.

A complete fusing system has been included which serves both as protection and as a short-circuit isolating means. Each section, of which there are 39, is locally fused, enabling the engineer to locate a short within only 12 chassis, rather than the total of 468.

An automatic voltage monitoring system may be used to test every d-c voltage at the rate of one per second. A meter movement relay signals any discrepancy from standard. Similarly, overheat thermostats detect any unfavorable temperature condition in the bays or mercury tanks.

Cooling for the power supply and central computer is provided by three blowers. Local cooling in the Uniservos is provided by small fans in each unit. The operating statistics of the UNIVAC are as follows:

Tape reading and recording:
Pulse density: 120 per inch
Tape speed: 108 inches per second
Input block size: 60 words: 720 characters
Tape width: ½ inch: 8 channels

Internal operations:
Memory capacity: 1,000 words; 12,000 characters
Memory construction: 100 mercury channels; 10 words/channel

Access time:
Average: 202 microseconds
Maximum: 404 microseconds

Word length:
12 characters
9 pulses
(include space between words = 7 pulses)

Basic pulse rate:
2.25 megacycles
Addition: 525 microseconds
Subtraction: 525 microseconds
Multiplication: 2,150 microseconds
Division: 3,890 microseconds
(All times shown include time for obtaining instructions and operands from memory)

Applications of UNIVAC

Types of problems for which UNIVAC is applicable

True to its name, Universal Automatic Computer, the UNIVAC system is capable of handling data processing or calculation in virtually all fields of human endeavor. It is particularly well suited to applications requiring large volumes of input or output data, or both.

For convenience and classification, applications of the UNIVAC will be treated under four headings: scientific, statistical, logistical, and commercial. The scientific problem usually, though not always, has relatively small amounts of input and output data, with emphasis on computation. The statistical problem has relatively large volumes of input data with a small volume of output data and simple processing procedures. The commercial and logistical problems both have relatively large amounts of input and output data with processing requirements varying from slight to relatively great. A number of problems in each of these four fields have been studied and found suited for solution on the UNIVAC system. Several in each field have actually been processed on the computer.

Scientific problems

A general-purpose matrix algebra routine designed to add, subtract, multiply, and reciprocate matrices of orders up to 300 has been prepared and applied to a number of matrices. Inverses have been calculated for three different matrices of orders 40, 50, and 44. The error matrices for the first two of these inverses also were calculated. In both, the largest error term was of the order of 10^{-8}. A triple product matrix was formed from component matrices ranging from 5 by 40 to 40 by 40. A check product was obtained by reversing the sequence of multiplications, verifying the original product to within 2 units in the 11th place. The computer time required for these calculations was 1 hour and 15 minutes to calculate the inverse of order 50, 45 minutes to determine its error matrix. The other calculations were proportionately shorter. In all of this work, magnetic tapes were used as temporary storage for the bulk of the matrix elements involved. The high speed of the tape reading units more than kept up with the computer's need for data. No mathematical checks, other than the over-all check mentioned, were included in the computation, the self-checking features of the system making these completely unnecessary.

A second computation—that of obtaining six different specific solutions to a system of 385 simultaneous equations—was completed in 27 minutes on the computer. The system of equations arose from a second order nonlinear differential equation of gas flow through a turbine. The error terms resulting from the substitution of the computed unknowns into the basic equation were of the order of 10^{-11}.

The third example is that of a 2-dimensional Poisson equation, using a 22 by 22 mesh. Each iteration required 13 seconds and produced a maximum separation of successive surfaces of the order of 10^{-8} after approximately 300 iterations.

Statistical problems

In the second major field of statistical computation, the Census problem has been a prime example. The Census problem produces a part of the Second Series Population on Tables for the 1950 Decennial Census.

The Second Series contains 30 types of tables covering the statistics of our population—age, sex, race, country of birth, education, occupation, employment, and income. These tables are to be compiled for every county, and for every city, rural farm, and rural nonfarm area within a county.

The preparation of these tables by the UNIVAC system requires three major steps:

1 Tabulation of each individual's characteristics by groups of about 7,000

2 Arranging these groups by cities, counties

3 Assembling from the tabulations the data required for each table

The raw data were prepared in the form of a punched card for each individual in the United States. The data from these enumeration cards are then transcribed onto magnetic tape. From these tapes, the computer processes the data sequentially through the three steps, producing output tapes from which the tables are printed on Uniprinters. The only manual operations encountered in this entire procedure are the handling of the original punched cards, mounting and demounting tape reel (the equivalent of 9,700 cards), and the removal of the printed tables from the Uniprinters.

The most important feature of the present procedure is the elimination of handling and sorting tremendous quantities of punched cards. Each handling of the card stacks is a source of potential error and delay. The UNIVAC memory permits the simultaneous accumulation of the 580 tallies which describe our population for each local area being studied by the UNIVAC system.

Commercial problems

In the commercial field, the UNIVAC system has handled premium billing for a life insurance company. This program produces premium notices, dividends, and commissions. In a particular example worked out, approximately 1,000,000 bills, 340,000 dividends, and 100,000 commissions have to be produced monthly. The necessary information for processing a particular policy is contained in 240 digits, or, in special cases, 480. This compactness is made possible by a logical system of 40 symbols, comprising both alphabetic and numeric characters, which denote over 90 definitions. The UNIVAC processes the policies as directed by the symbols, policy dates, and policy numbers.

The problem includes inserting over 250,000 changes each month before further handling is done. After this step, the policies to be processed are selected from a file of 1,500,000 items. Next, a list is produced of the cases which have symbols indicating that special notices must be sent to the policyholders. Following the calculation of dividends and commissions, additional lists are produced: one group contains information pertaining to commissions and agents; another contains information regarding dividends; and finally, there is a listing of option changes for later insertion into the policy files. Policies requiring premium notices are then edited and the notices are automatically printed from the data contained on magnetic tapes.

The UNIVAC time needed for a program of this proportion is about 135 hours a month. The average computer time per policy processed is less than 0.5 second. The average time for all change insertions, printing, calculations, and unityping is 9 seconds per item.

Logistical problems

In the field of logistics, five major studies have been conducted, four of these resulting in actual problems executed on the computer.

The first is the type of computation in which the basic purpose is to determine quantitively whether a given operational or mobilization plan can be logistically supported. The ultimate desired is to find, by calculation, the optimum program for carrying out such plans. At the time of writing, only a small model has been actually run on UNIVAC, but full size models will be run within the next few weeks. Two computations have been executed, one a set of three tables of thousands of lines each, giving a detailed breakdown of machine deployment, fuel requirements, and overhaul requirements. The other problem was a computation of the amounts of critical raw materials required to construct a given number of each type of equipment, these requirements being phased by quarters over a 2-year period. The fourth problem, which was actually computed, was a sample of a similar calculation in which every pound of critical raw material required each month for the ultimate construction of a complete building program was computed.

The UNIVAC program which was prepared is capable of accommodating every type of equipment, individually tailored construction schedules, detailed bills of materials running into the millions of items and of determining the actual amounts of alloy elements based on thousands of tables of percentages for the many alloys employed. The demonstration showed that this computation for 400 pieces of equipment of a given type could be executed in three hours of computer time. The last problem in this field has not yet been run, but the study has shown that the entire gamut of stock control for a large supply office can be covered by the computer in approximately 3 weeks time.

This program involves the maintenance of stock balances of hundreds of thousands of stock items for many service points and provides for the preparation of stock transfer orders, purchase requisitions, critical lists and summary reports.

Performance record of the UNIVAC

Acceptance tests

The Acceptance Tests, prepared jointly by the Bureau of Standards and Bureau of Census, are fully discussed in the following paper by Dr. Alexander and Mr. McPherson.[1] However, a few comments

[1] Paper not included in this book. See McPherson and Alexander [1951].

concerning them from the engineering point of view are appropriate.

The Census computer was given two tests; the first, a test of its computational ability; the second, a test of its input-output system which particularly stressed the tape reading and recording abilities.

The Central Computer Acceptance Test A consisted of two parts. During Part 1, every available internal operation, except input-output operations, was performed. Among these operations were addition, subtraction, comparisons, division, and three different types of multiplication operations. Each of the arithmetic operations handled a pair of 11-decimal digit quantities. Altogether there were about 2,500 operations in the routine, yet the entire routine required only 1.26 seconds to do. The routine was performed 808 times in 17 minutes making a total of about 2,000,000 operations in all.

The second part of Test A included the solution of a heat distribution equation, a short routine involving the input-output device and a sorting routine. The sorting routine arranged ten numerical quantities each containing 12 decimal digits in correct numerical order in about 0.2 second. All three routines took a total of 1½ minutes to perform. They were performed twice for each test and when added to Part 1 made a total of 20 minutes for unit test A.

The Acceptance Test B examined the input-output tape devices (Uniservos). During the first part of Test B, 2,000 blocks or about 1.4 million digits, which included every available character (numeric and alphabetic) were recorded on a tape and then read back into the computer with the tape moving backward. The information read back was then compared with the original data read out. The recording operation required about 4 minutes while reading back and comparison required about 8 minutes. The second part of Test B consisted of recording and reading over one spot of tape for 700 passes in order to determine the readability of tape as it wears. This test required 13 minutes and when combined with Part 1, made a total of approximately 25 minutes for Test B. This test was repeated 19 times.

The first test run passed in 6.6 hours (minimum theoretical time: 6.0 hours) and the second test was passed in 9.47 hours (minimum theoretical time: 7.45 hours). Of the 2.02 hours down time, 1.45 hours were accumulated at one time with the remaining 0.58 hours spread over the rest of the test.

The Uniprinter test required that a block of information (60 words) be printed 200 times in tabular form. The minimum time for printing was five hours. The test was passed in 6.16 hours.

The card-to-tape test required that ten good reels of tape be produced in 12 hours. There were certain restrictions as to reading accuracy and other criteria of reproducing ability which defined "good" reels. In 10 hours, the converter had prepared over 15 reels, 14 reels had been tested, 11 of the 14 were found satisfactory and the converter was accepted for payment.

Although the test was run on only one of two converters, the Bureau of Census put both card-to-tape machines into operation and after six months of use, the acceptance test was run on the second card-to-tape converter. This test differed to some extent from the first test in that the Census Bureau was satisfied with the reading ability of the machines and did not require a digit-by-digit verification of the information. However, a new stipulation was added that, after the engineers had checked the converter out preparatory to running the test, the converter was to be used in actual operation for eight hours before doing the remainder of the test with no engineering intervention between the two portions of the test. The first part was run on Friday, October 5, 1951; the device remained idle Saturday and Sunday and was turned on Monday morning to complete the test. It passed with flying colors, preparing ten acceptable reels (out of ten reels) plus two decks of check cards in slightly less than 7 hours. Both card-to-tape converters now are in Washington and the remainder of the system is in operation by the Bureau of the Census on the Eckert-Mauchly premises in Philadelphia.

Reliability and factors affecting performance

The first UNIVAC system now has been operating for approximately 8 months. In that time, much has been learned about how UNIVACs should be operated and maintained. The situation has been somewhat complicated by having to shake down the equipment while in the customer's possession; that is, there were certain faults in the system from both engineering and production standpoints which could only become apparent in the course of time and under actual operation conditions. For example, weak tubes or faulty solder joints did not reveal their presence at the time of installation. Another type of difficulty only became apparent under certain duty cycle conditions imposed by various types of problems. Because only certain problems present this particular duty cycle, these troubles remained in the machine causing intermittent stoppages until they could be tracked down.

Patient isolation and elimination of such problems, most of which have occurred only with conditions of operation infrequently encountered, is a powerful, though sometimes painful proving ground for the engineering group charged with such responsibility. The experience and depth of judgment acquired by such a group in the course of performing such work have become unmistakably apparent in the already noted improved performance of following UNIVACs and generally advanced ability to predict

and realize performance in any large scale and complex apparatus of the same character.

Some of the troubles encountered are interesting to study in detail. On a rather complicated routine requiring the use of a number of Uniservos, all ran smoothly for 15 minutes. At that time, one of the Uniservos executing a backward read somewhere in the middle of the reel, did not stop at the end of the block but continued to run until it ran off the end of the tape. After much work, it was shown that a cycling unit signal was being overloaded because it was being used both by a multiplication instruction and the backward read which were occurring simultaneously. The input precessor loop was cleared as a result and the count of the pulses coming off the tape was thereby lost. Once the trouble was found, it was simple to remedy.

Another rather interesting case occurred intermittently over an extended period. Normally when reading out of the memory, the contents should not be cleared. Occasionally, however, reading from the memory also caused the contents to be cleared. As the trouble only remained for a period of seconds or, at most, a few minutes, it was somewhat difficult to localize. Of course, parasitic oscillations of some sort were suspected and, in fact, the trouble was traced to the actual source on a logical basis; but the source, a high power cathode follower, showed no evidence of oscillation. Before the problem was remedied, various combinations of parasitic suppressors were tried; the trouble would vanish for perhaps a week and then return. The oscillation finally cropped up during a maintenance shift, was found to be in the suspect tube at 100 megacycles and was eliminated rather easily.

Other types of troubles that have occurred include intermittent parasitic oscillations in other circuits, bounce in Uniservo relay circuits, various mechanical problems in Uniservos, time constants not consistent with the longest duty cycle signals, and various types of noise in the input circuits. The tubes, which initially were bothersome, have now stabilized to the point where two tubes per week (on the average) stop the computer during computation.

All of the above troubles and others not discussed here have contributed to lost computing time on the UNIVAC. However, they cannot influence future operation because the reasons for them have been found and eliminated. The fact that these troubles will not occur in future UNIVACs cannot be emphasized too strongly.

Under a contract with the Bureau of Census, Eckert-Mauchly Computer Corporation maintains the Census installation. This system is operated 24 hours a day, seven days a week, except for four 8-hour preventive maintenance shifts each week. This allows approximately 32 hours for regular maintenance and 136 hours for operation or 21 and 79 per cent respectively. Table 1 shows the engineering time spent on the computer system during typical weeks of operation. The figures are given both in hours and percentages. Both nonscheduled engineering time as well as preventive maintenance time are shown. The sum of the two gives the total engineering time spent on the computer per week. It should be noted that this is actual engineering time and does not include time that the computer may have been shut down while waiting for an engineer to report. According to our maintenance contract, this must be within a half hour during regular working hours and within two hours at all other times. Attention should be given to the fact that the preventive maintenance time does not total exactly 32 hours each week. This is due in part to a half-hour period each morning devoted to checking and cleaning the mechanical portions of Uniservos. It is expected that this work will be taken over by the UNIVAC operators since the procedures and the techniques involved are quite simple.

In addition, one extra shift was required the week ending June 3 and three extra shifts the week ending October 7, 1951. These shifts were required to incorporate engineering changes which had been developed over a period of time and could not be incorporated in the equipment during the normal preventive main-

Table 1

Week ending 1951	*Nonscheduled engineering*		*Preventive maintenance*		*Total engineering time*		*Percentage of nonscheduled engineering*
	Hours	*Per Cent*	*Hours*	*Per Cent*	*Hours*	*Per Cent*	
June 3	18.9	11.3	40	23.8	58.9	35.1	14.8
26	20.5	12.2	34	20.2	54.5	32	15.3
July 14	14.7	8.8	33	19.6	47.7	28	10.9
21	19.4	11.6	34.5	20.5	53.9	32	14.5
28	39.2	23.3	34.5	20.5	73.7	43.8	29.4
Aug. 4	26.2	15.6	33	19.6	59.2	35.2	19.4
Sept. 2	28.8	17.1	34.5	20.5	63.3	37.7	21.6
9	16.1	9.6	34.5	20.5	50.6	30	12.1
16	22.6	13.5	33	19.6	55.6	33	16.7
23	42.3	25.2	34.5	20.5	76.8	45.7	31.7
30	21.8	13.0	34.5	20.5	56.3	33.5	16.3
Oct. 7	15.9	9.5	56	33.3	71.9	42.8	14.2
14	14.0	8.3	34.5	20.5	48.5	28.9	10.5
21	10.4	6.2	34.5	20.5	44.9	26.7	7.8
28	20.8	12.4	33	19.6	53.8	32	15.4
Nov. 4	40.4	24.0	34.5	20.5	74.9	44.6	30.3
11	10.1	6.0	34.5	20.5	44.6	26.5	7.6
18	30.5	18.2	34.5	20.5	65	38.7	22
25	13.7	8.2	34.5	20.5	48	28.6	10
Dec. 2	14.8	8.7	34.5	20.5	49.3	29.3	12.6
9	19.6	11.7	34.5	20.5	54.1	32.2	14.7

tenance time. The nonscheduled engineering time has varied from as little as 10.1 hours or 6 per cent to 42.3 hours or 25 per cent. The last column in the Table shows the amount of nonscheduled engineering time as compared to the allowable operating time (total time less preventive maintenance time). Here there is a variation of from 7.6 to 31.7 per cent and an average for the weeks shown of 16.9 per cent. It is believed that these figures, while good for the first months of operation of a new piece of equipment, will show definite improvement over the next year.

Although the opportunity to prove or disprove the following theory of operation has not presented itself, it is believed logical that optimum use of the UNIVAC equipment might be obtained by means of scheduling preventive maintenance only at such times as it is indicated in the judgment of competent operators. In other words, there are many occasions preceding a scheduled maintenance shift when the system is performing very well. At such times, it is extremely inefficient to shut down the operation in order to provide maintenance. For many reasons, however, it has been impossible to operate and maintain the first system in this way. It is hoped that such operation will be possible in following installations.

It should be realized that the UNIVAC system requires a supervisor of the same caliber as the one required for a large punched card installation. However, the large group of operating personnel would be replaced by a small group of well-trained extremely competent people thoroughly familiar with the details of the computer and associated equipment. The time spent in providing a high degree of training for these people is more than repaid in increased operating efficiency and consequently higher work output. For example, situations arise in the course of running a problem where a correct operational decision can save hours of elapsed computation. Also, a competent operator will recognize malfunctions sufficiently early to prevent serious delays. He is capable of deciding whether to continue with machine operation or to stop to diagnose. The second UNIVAC system which is ready for installation in Washington, will be operated by a group of engineers who have been trained in operation and maintenance. This procedure, it is believed, will result in the UNIVAC system being of maximum benefit to the Air Comptroller's Office.

Evaluation of UNIVAC design

Checking features

Maintenance of the UNIVAC has been vastly simplified by use of duplicate arithmetic and control equipment and other checking methods. Many factors which would have led to undetected errors have, by virtue of duplication, immediately stopped the computer. Although checking by means of inverse operations can provide operational checks on the arithmetic circuits, there is some question as to whether it provides as good a check as duplication. However, in connection with odd-even codes, it may conceivably be comparable. It should be remembered, however, that this is from an operational standpoint and not a maintenance standpoint. When the control equipment is considered it is difficult to visualize a check that is as good as duplicated equipment. Other checks that are utilized in UNIVAC include the periodic memory check, intermediate line function table checker, function table output checker, memory switch checker, and 720 checker.

As explained earlier in the paper, the periodic memory check is accomplished by reading out of all memory channels sequentially and performing an odd-even check on each digit as it passes through the high speed bus amplifier. The period at which the check is repeated may be varied over a large interval. At present, it is set at 5 seconds, the check taking 52 milliseconds or about 1 per cent of the computing time.

The function table has a check at the very input by bringing in the check pulse in each character so that if an odd-even error occurs between the control register and the static register, no order will be set up and the computer will grind to a halt! If the input sets up properly but an error occurs farther on in the table, but not ahead of the intermediate lines (the linear set into which the input combinations are decoded), the error is caught at this point. The intermediate lines are broken into groups in such a way that an error is indicated when more than one line is set up in one group or the entire set. There is an exception to this in some groups where no error is indicated by this checker if more than one line is set up within the group.

This has been allowed only in those cases where it has been shown that setting up two or more lines will cause some other checker or checkers to indicate the trouble.

If the error occurs beyond the intermediate lines, the output checker then comes into play. This checker makes an odd-even count on the number of gates used on each instruction: dummy lines having been added so that the count is normally always odd.

The memory switch or tank selector checker ensures that one and only one memory channel is selected on any instruction. It checks each of the two digit positions separately indicating which if either, is in error.

The 720 checker counts the digits coming off the tape and if there are either more or less than 720 in one block, the computer stops; by examining the indicators on the supervisory control console, the operator can determine the number of digits actually

read. By means of some rather simple manipulations, the operator can then reread the block without losing his place in the routine; and if the information is then read correctly, he may again start the computer on the routine. The same procedure may be followed if an odd-even error is made in reading from the tape.

Many checks other than those mentioned before have been built into the UNIVAC. On the basis of operating experience, the engineers cannot recommend too strongly the use of built-in checking facilities. All in all, the faith that can be put into results obtained from an unchecked computer comparable in size to UNIVAC is in the writers' opinion exceedingly low.

More than this, however, the methods by which the UNIVAC is checked have been of extreme usefulness in trouble shooting. The duplication of circuits has amply repaid the increase of space and the number of components required by this checking system.

General comments

After evaluating UNIVAC performance over a period of eight months, the over-all picture of the UNIVAC design, in the minds of its designers, is extremely good. Certain phases of its design exceeded expectations, while of course, other phases were somewhat disappointing. The first eight months of actual operation have taught more than years of experimentation with laboratory models. Many improvements have already been conceived of this experience and are continuing daily to increase reliability.

The other major factor influencing computer design, cost, has been duly considered in the UNIVAC design; and it is being met with plans for a continuing full-scale production of UNIVAC systems. As the production techniques are developed concurrently with the engineering design details, the UNIVAC becomes the realization of a hope which has long been in the minds of its designers: An economical, completely reliable commercial computer for performing the routine mental work of the world much as automatic machinery has taken over the routine mechanical work of the manufacturer.

References

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