Chapter 17

IBM 650 instruction logic[1]

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The basic IBM 650 is a magnetic drum (10, 0, 0)[2] decimal computer with one-plus-one address instruction logic. It has a storage of 1000 or 2000 10-digit words (plus sign) with addresses 0000–0999 or 0000–1999. More extended versions of the equipment have built-in floating point arithmetic and index accumulators, but the basic machine will be described here. There are three arithmetic registers in addition to the standard program register and program counter. All information from the drum to the arithmetic unit passes through a signed 10-digit *distributor*. A twenty-digit *accumulator* is divided into a lower and upper part, each of 10 digits with sign. Each of these is addressable (distributor 8001, lower accumulator 8002, and upper accumulator 8003). Each accumulator may be cleared to zero separately (in IBM 650 terminology, "reset"). The entire 20-digit register can be considered as a unit, or each part separately (but affecting the other in case of carries). The 10-digit instruction is broken down into the following form:

10	9	8	7	6	5	4	2	3	1	0
Op. Code		Data Address				Next Instruction Address				Sign

One particular instruction, Table Look-Up, allows automatic table search for one particular element in a table, which can be stored with a corresponding functional value. Input-output is via 80-digit numerical punched cards. An "alphabetic device" allows limited alphabetical entry on cards. Only certain 10-word groups on the magnetic drum are available for input and output. The following information is taken from an IBM 650 manual [Type 650, Magnetic Drum Data-Processing Machine Manual of Operations]. Much of the input-output is handled via board wiring, which is not described in detail below. The two-digit pair represents the machine code. The BRD (Branch on Digit) operation is used with special board wiring to tell when certain specific card punches exist.

[1]In E. M. Grabbe, S. Ramo, and D. E. Wooldridge (eds.), "Handbook of Automation, Computation, and Control," vol. 2, chap. 2, pp. 93–98, John Wiley & Sons, Inc., New York, 1959.

[2]Carr's triplet notation for: fractional significant digits, digits in exponent, and digits to left of radix point.

Input-output instructions

70 RD (Read). This operation code causes the machine to read cards by a two-step process. First, the contents of the 10 words of read buffer storage are automatically transferred to one of the 20 (or 40) possible 10-word groups of read general storage. The group selected is determined by the D address of the Read instruction. Secondly, a card is moved under the reading brushes, and the information read is entered into buffer storage for the next Read instruction.

71 PCH (Punch). This operation code causes card punching in two steps. First the contents of one of the 20 (or 40) possible 10-word groups of punch storage are transferred to punch buffer storage. The group selected is specified by the D address of the Punch instruction. Secondly, the card is punched with the information from buffer storage.

69 LD (Load Distributor). This operation code causes the contents of the D address location of the instruction to be placed in the distributor.

24 STD (Store Distributor). This operation code causes the contents of the distributor with the distributor sign to be stored in the location specified by the D address of the instruction. The contents of the distributor remain undisturbed.

Addition and subtraction instructions

10 AU (Add to Upper). This operation code causes the contents of the D address location to be added to the contents of the upper half of the accumulator. The lower half of the accumulator will remain unaffected unless the addition causes the sign of the accumulator to change, in which case the contents of the lower half of the accumulator will be complemented. Also, the units position of the upper half of the accumulator will be reduced by one.

15 AL (Add to Lower). This operation code causes the contents of the D address location to be added to the contents of the lower half of the accumulator. The contents of the upper half of the accumulator could be affected by carries.

11 SU (Subtract from Upper). This operation code causes the contents of the D address location to be subtracted from the

contents of the upper half of the accumulator. The contents of the lower half of the accumulator will remain unaffected unless the subtraction causes a change of sign in the accumulator, in which case the contents of the lower half of the accumulator will be complemented. Also, the units position of the upper half of the accumulator will be reduced by one.

16 SL (Subtract from Lower). This operation code causes the contents of the D address location to be subtracted from the contents of the lower half of the accumulator. The contents of the upper half of the accumulator could be affected by carries.

60 RAU (Reset and Add into Upper). This operation code resets the entire accumulator to plus zero and adds the contents of the D address location into the upper half of the accumulator.

65 RAL (Reset and Add into Lower). This operation code resets the entire accumulator to plus zero and adds the contents of the D address location into the lower half of the accumulator.

61 RSU (Reset and Subtract into Upper). This operation code resets the entire accumulator to plus zero and subtracts the contents of the D address location into the upper half of the accumulator.

66 RSL (Reset and Subtract into Lower). This operation code resets the entire accumulator to plus zero and subtracts the contents of the D address location into the lower half of the accumulator.

Accumulator store instructions

20 STL (Store Lower in Memory). This operation code causes the contents of the lower half of the accumulator with the accumulator sign to be stored in the location specified by the D address of the instruction. The contents of the lower half of the accumulator remain undisturbed.

It is important to remember that the D address for all store instructions must be 0000–1999. An 8000 series D address will not be accepted as valid by the machine on any of the store instructions.

21 STU (Store Upper in Memory). This operation code causes the contents of the upper half of the accumulator with the accumulator sign to be stored in the location specified by the D address of the instruction. If STU is performed after a division operation, and before another division, multiplication, or reset operation takes place, the contents of the upper accumulator will be stored with the sign of the remainder from the divide operation (Op-Code 14). The contents of the upper half of the accumulator remain undisturbed.

22 STDA (Store Lower Data Address). This operation code causes positions 8–5 of the distributor to be replaced by the contents of the corresponding positions of the lower half of the accumulator. The modified word in the distributor with the sign of the distributor is then stored in the location specified by the D address of the instruction.

23 STIA (Store Lower Instruction Address). This operation code causes positions 4–1 of the distributor to be replaced by the contents of the corresponding positions of the lower half of the accumulator. The modified word in the distributor with the sign of the distributor is then stored in the location specified by the D address of the instruction. The contents of the lower half of the accumulator remain unchanged, and the sign of the accumulator is not transferred to the distributor. The modified word remains in the distributor upon completion of the operation.

Absolute value instructions

17 AABL (Add Absolute to Lower). This operation code causes the contents of the D address location to be added to the contents of the lower half of the accumulator as a positive factor regardless of the actual sign. When the operation is completed, the distributor will contain the D address factor with its actual sign.

67 RAABL (Reset and Add Absolute into Lower). This operation code resets the entire accumulator to zeros and adds the contents of the D address location into the lower half of the accumulator as a positive factor regardless of its actual sign. When the operation is completed, the distributor will contain the D address factor with its actual sign.

18 SABL (Subtract Absolute from Lower). This operation code causes the contents of the D address location to be subtracted from the contents of the lower half of the accumulator as a positive factor regardless of the actual sign. When the operation is completed, the distributor will contain the D address factor with its actual sign.

68 RSABL (Reset and Subtract Absolute into Lower). This operation code resets the entire accumulator to plus zero and subtracts the contents of the D address location into the lower half of the accumulator as a positive factor, regardless of the actual sign. When the operation is completed, the distributor will contain the D address factor with its actual sign.

Multiplication and division

19 MULT (Multiply). This operation code causes the machine to multiply. A 10-digit multiplicand may be multiplied by

a 10-digit multiplier to develop a 20-digit product. The multiplier must be placed in the upper accumulator prior to multiplication. The location of the multiplicand is specified by the D address of the instruction. The product is developed in the accumulator beginning in the low-order position of the lower half of the accumulator and extending to the left into the upper half of the accumulator as required.

14 DIV (Divide). This operation code causes the machine to divide without resetting the remainder. A 20-digit dividend may be divided by a 10-digit divisor to produce a 10-digit quotient. In order to remain within these limits, the absolute value of the divisor must be *greater than* the absolute value of that portion of the dividend that is in the upper half of the accumulator. The entire dividend is placed in the 20-position accumulator. The location of the divisor is specified by the D address of the divide instruction.

64 DIV RU (Divide and Reset Upper). This operation code causes the machine to divide as explained under operation code 14 (DIV). However, the upper half of the accumulator containing the remainder with its sign is reset to zeros.

Branching instructions (decision operations)

44 BRNZU (Branch on Non-Zero in Upper). This operation code causes the contents of the upper half of the accumulator to be examined for zero. If the contents of the upper half of the accumulator is nonzero, the location of the next instruction to be executed is specified by the D address. If the contents of the upper half of the accumulator is zero, the location of the next instruction to be executed is specified by the I address. The sign of the accumulator is ignored.

45 BRNZ (Branch on Non-Zero). This operation code causes the contents of the entire accumulator to be examined for zero. If the contents of the accumulator is nonzero, the location of the next instruction to be executed is specified by the D address. If the contents of the accumulator is zero, the location of the next instruction to be executed is specified by the I address. The sign of the accumulator is ignored.

46 BRMIN (Branch on Minus). This operation code causes the sign of the accumulator to be examined for minus. If the sign of the accumulator is minus, the location of the next instruction to be executed is specified by the D address. If the sign of the accumulator is positive, the location of the next instruction to be executed is specified by the I address. The contents of the accumulator are ignored.

47 BROV (Branch on Overflow). This operation code causes the overflow circuit to be examined to see whether it has been set. If the overflow circuit is set, the location of the next instruction to be executed is specified by the D address. If the overflow circuit is not set, the location of the next instruction to be executed is specified by the I address.

90-99 BRD 1-10 (Branch on 8 in Distributor Position 1-10). This operation code examines a particular digit position in the distributor for the presence of an 8 or 9. Codes 91–99 test positions 1–9, respectively, of the test word; code 90 tests position 10. If an 8 is present, the location of the next instruction to be executed is specified by the D address. If a 9 is present, the location of the next instruction to be executed is specified by the I address. The presence of other than an 8 or 9 will stop the machine.

Shift instructions

30 SRT (Shift Right). This operation code causes the contents of the entire accumulator to be shifted right the number of places specified by the units digit of the D address of the shift instruction. A maximum shift of nine positions is possible. A data address with units digit of zero will result in no shift. All numbers shifted off the right end of the accumulator are lost.

31 SRD (Shift Round). This operation causes the contents of the entire accumulator to be shifted right the number of places specified by the units digit of the D address of the instruction. A 5 is added (−5 if the accumulator is negative) in the twenty-first (blind) position of the amount in the accumulator. A data address units digit of zero will shift 10 places right with rounding.

35 SLT (Shift Left). This operation code causes the contents of the entire accumulator to be shifted left the number of places specified by the units digit of the D address of the instruction. A maximum shift of nine positions is possible. A data address with a units digit of zero will result in no shift. All numbers shifted off the left end of the accumulator are lost. However, the overflow circuit will not be turned on.

36 SCT (Shift Left and Count). This operation code causes (1) the contents of the entire accumulator to be shifted to the left until a nonzero digit is in the most significant place, (2) a count of the number of places shifted to be inserted in the two low-order positions of the accumulator. This instruction is to aid fixed-point scaling.

Table look-up instructions

84 TLU (Table Look-up). This operation code performs an automatic table look-up using the D address as the location of

the first table argument and the I address as the address of the next instruction to be executed. The argument for which a search is to be made must be in the distributor. The address of the table argument equal to, or higher than (if no equal exists) the argument given is placed in positions 8–5 of the lower accumulator. The search argument remains, unaltered, in the distributor.

Miscellaneous instructions

00 No-Op (No Operation). This code performs no operation. The data address is bypassed, and the machine automatically refers to the location specified by the instruction address of the **No-Op** instruction.

01 Stop. This operation code causes the program to stop provided the *programmed* switch on the control console is in the stop position. When the *programmed* switch is in the run position the 0I code will be ignored and treated in the same manner as **00 (No-Op)**.

References

Type 650 Magnetic Drum Data-Processing Machine Manual of Operations; HughE54; SerrR62.